INTERSIL

A Precision Waveform Generator and Voltage Controlled Oscillator

DESCRIPTION

The 8038 Waveform Generator is a monolithic integrated circuit, capable of producing sine, square, triangular, sawtooth and pulse waveforms of high accuracy. The frequency (or repetition rate) can be selected externally over a range from less than 1/100 Hz to more than 1/2 MHz and is highly stable over a wide temperature and supply voltage range. Frequency modulation and sweeping can be accomplished with an external voltage and the frequency can be programmed digitally through the use of either resistors or capacitors. The Waveform Generator utilizes advanced monolithic technology, such as thin film resistors and Schottky-barrier diodes.

THEORY OF OPERATION

A block-diagram of the waveform generator is shown in Figure 1. An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, then the capacitor is charged with a current I. Thus the voltage across the capacitor rises linearily with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts anew.

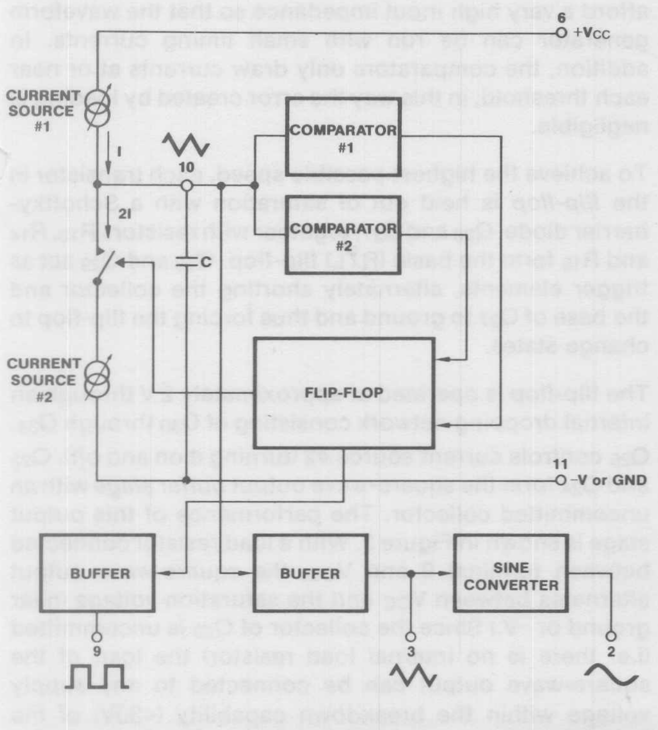

FIGURE 1. BLOCK-DIAGRAM OF WAVEFORM GENERATOR.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

THE DETAILED CIRCUIT DIAGRAM (FIGURE 2)

The *current sources* are formed by transistors Q_1 through Q_{13}. A reference voltage is formed by a resistance voltage divider (R_1, R_2) at pin 7; this reference voltage is therefore a precise fraction of the supply voltage (set at 80%). If frequency modulation or sweep is not used, pins 7 and 8 are connected together for best temperature performance.

Q_1 acts as an emitter follower, so that the impedance at pin 8 is very high. Two lateral pnp transistors (Q_2 and Q_3) receive their base signal from the emitter of Q_1. These two transistors carry a current which is determined by the base voltage and the resistance connected in series with the emitters, i.e. the two external resistors.

Notice that cancellation of base-emitter voltage-drops takes place in this circuit. The emitter-voltage of Q_1 is *lower* by one V_{BE} compared to the reference voltage, but the voltages at pins 4 and 5 are *higher* by one V_{BE} compared to that of the emitter of Q_1. Therefore, the voltages at pins 8, 5 and 4 are equal and the two currents are given by

$$I = \frac{V_{CC} - V_{ref}}{R_{ext}} = \frac{R_1 \times V_{CC}}{(R_1 + R_2)\, R_{ext}} = \frac{0.2\, V_{CC}}{R_{ext}}$$

To allow a wide current range, npn transistors (Q_4, Q_5) have been added to form composite pnp equivalents. In this way each current source can deliver up to 10 mA.

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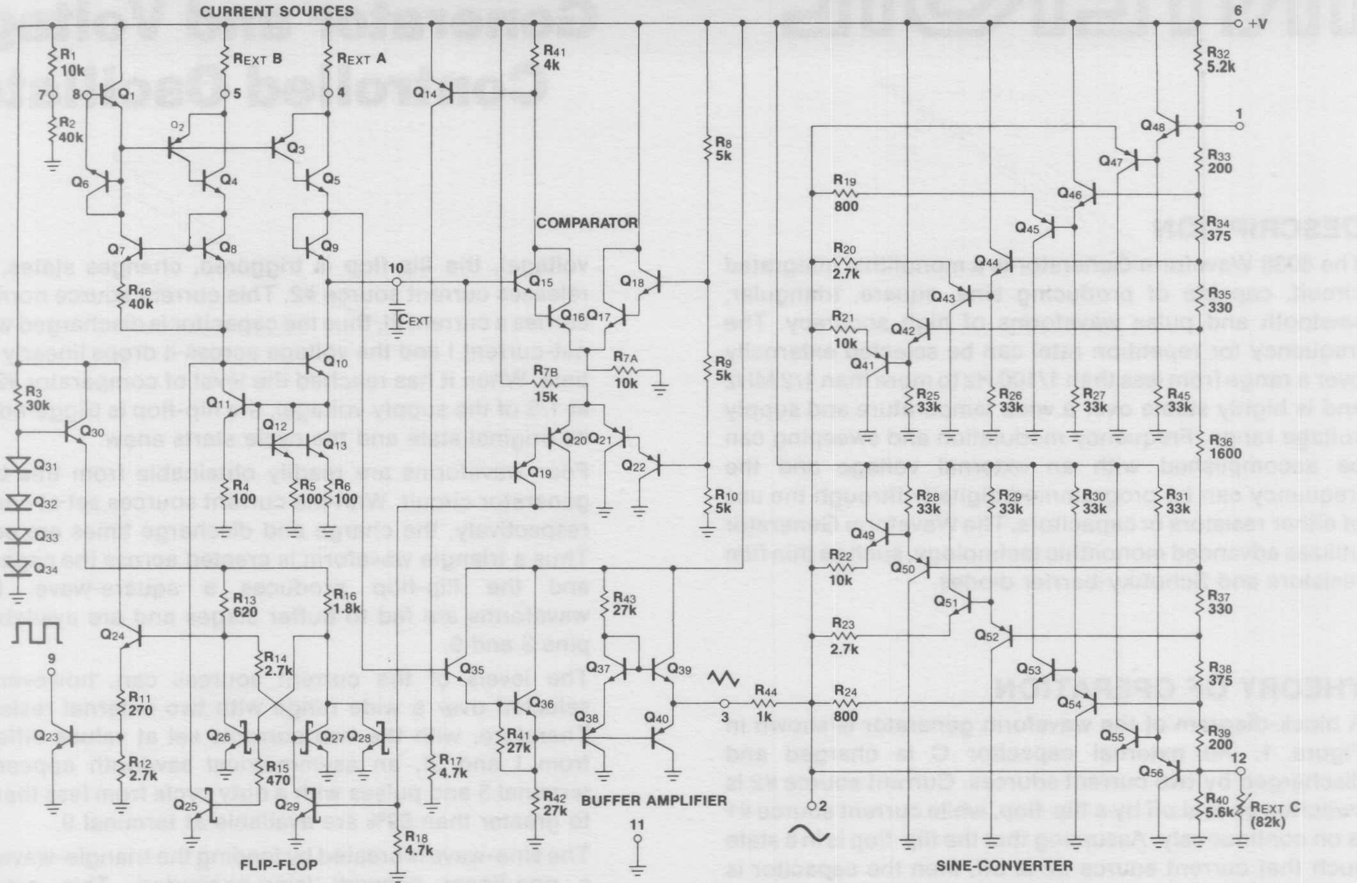

FIGURE 2. DETAILED CIRCUIT DIAGRAM OF WAVEFORM GENERATOR.*

A small amount of current is returned to the bases of Q_2 and Q_3 through the diode-biased transistor connection of Q_7 and Q_8. This current is necessary to provide sufficient base current for the lateral pnp transistors. The diode Q_6 acts as a start-up current path.

The transistors Q_{10} through Q_{13} are connected as a Wilson current source with a 2:1 current ratio. As long as the collector of Q_{11} is undisturbed, the collector of Q_{10} will sink a current which has precisely twice the magnitude of that flowing into terminal 5. When the collector of Q_{11} is shorted to ground by the flip-flop (Q_{25}), the collector current in Q_{10} ceases to flow.

The two *comparators* are formed by transistors Q_{15} through Q_{22}. Each comparator consists of a differential Darlington pair. The two levels are derived from a precision voltage divider (R_8, R_9, R_{10}) with three equal resistance values. As long as the voltage across capacitor C is below 2/3 of the supply voltage, the entire current in the npn differential pair flows through Q_{17} and Q_{18}. At precisely 2/3 V_{CC} this current switches to Q_{15} and Q_{16}. This in turn causes a current to flow in Q_{14} which changes the state of the flip-flop.

The identical response is obtained from the pnp differential Darlington pair Q_{19} through Q_{22}. As long as the voltage across the capacitor is larger than 1/3 V_{CC}, only Q_{21} and Q_{22} carry current. At 1/3 V_{CC}, Q_{19} and Q_{20} turn on and change the state of the flip-flop through Q_{29}.

Both comparators are made from Darlington pairs to afford a very high input impedance so that the waveform generator can be run with small timing currents. In addition, the comparators only draw currents at or near each threshold; in this way the error created by loading is negligible.

To achieve the highest possible speed, each transistor in the *flip-flop* is held out of saturation with a Schottky-barrier diode. Q_{26} and Q_{27}, together with resistors R_{13}, R_{14} and R_{16} form the basic (RTL) flip-flop. Q_{28} and Q_{29} act as trigger elements, alternately shorting the collector and the base of Q_{27} to ground and thus forcing the flip-flop to change states.

The flip-flop is operated at approximately 2 V through an internal dropping network consisting of Q_{30} through Q_{34}. Q_{25} controls current source #2 (turning it on and off). Q_{23} and Q_{24} form the square-wave output *buffer stage* with an uncommitted collector. The performance of this output stage is shown in Figure 3. With a load resistor connected between terminal 9 and V_{CC}, the square-wave output alternates between V_{CC} and the saturation voltage (near ground or −V.) Since the collector of Q_{23} is uncommitted (i.e. there is no internal load resistor) the load of the square-wave output can be connected to any supply voltage within the breakdown capability (<30V) of the transistor.

* Connections shown are for operation from a single-ended supply. For operation from a dual supply, the connections shown to ground (Pin 11) would be taken to V−.

FIGURE 3. PERFORMANCE OF THE SQUARE-WAVE OUTPUT (PIN 9).

Notice that the flip-flop is triggered only on the right-hand side, while the outputs are taken from the left-hand side. In this way the flip-flop is forced to change state *before* it is allowed to act on the current source, avoiding potential hang-up or false triggering problems.

Q_{35} through Q_{40} are connected as the *triangle output buffer stage.* The triangle waveform is picked up at a potential one V_{BE} above that carried by the capacitor. A Darlington emitter follower (Q_{35}, Q_{36}) is used to provide a high impedance. Thus, at the emitter of Q_{36}, the potential of the waveform is one V_{BE} below that of the capacitor. The subsequent Class-B output stage formed by Q_{39} and Q_{40} and their biasing chain Q_{37}, Q_{38} shift the dc level up by one V_{BE} so that the waveform of pin 3 has the same dc potential and magnitude as that of the capacitor. Since the trigger thresholds are chosen at 1/3 and 2/3 V_{CC}, the average (or dc) potential of the triangle is precisely in the center of the supply voltage and the peak-to-peak amplitude is exactly 1/3 of the supply voltage. Operating the waveform generator from a dual power-supply with equal positive and negative voltages puts the average of the triangle at ground level.

The performance of the triangle output stage is shown in Figure 4. Notice that the load can be connected to either grond, +V or –V.

The remainder of the circuitry, transistors Q_{41} through Q_{56}, is used to create the *sine-wave.* Eight reference voltages are provided by the resistance voltage divider R_{32} through R_{40}, symmetrically about the center point between the positive and negative supply voltage. As the triangle wave passes the level of the first reference voltage in the positive direction, Q_{41} starts conducting (the base-emitter voltages of an npn and a pnp transistor are nulled out so that the reference voltage appears both at the base of Q_{42} and the emitter of Q_{41}). Thus, at this voltage level, the triangle wave is attenuated by the ratio of R_{44} to R_{21}. At the higher voltage levels additional and decreasing resistances become active. This non-linear attenuator, therefore, shapes the triangle-wave into a sine-wave. An identical attenuator (with reversed polarity) is provided for the negative half of the waveform.

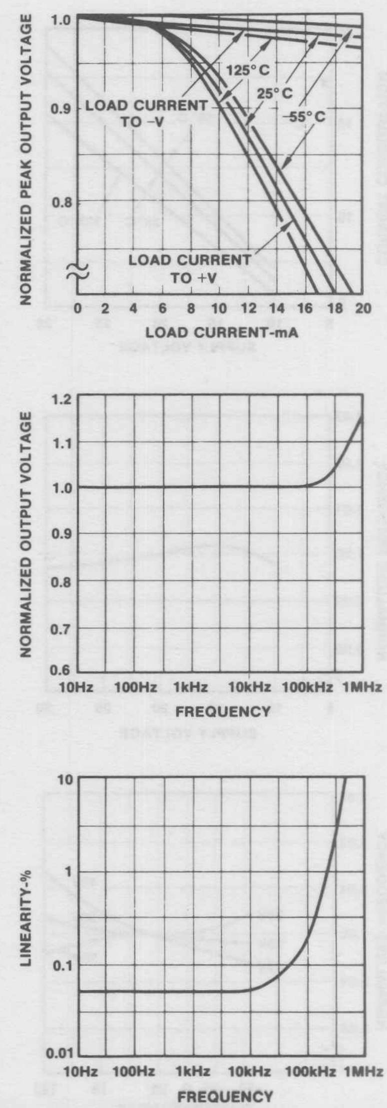

FIGURE 4. PERFORMANCE OF TRIANGLE-WAVE OUTPUT.

FIGURE 5. PERFORMANCE OF SINE-WAVE OUTPUT.

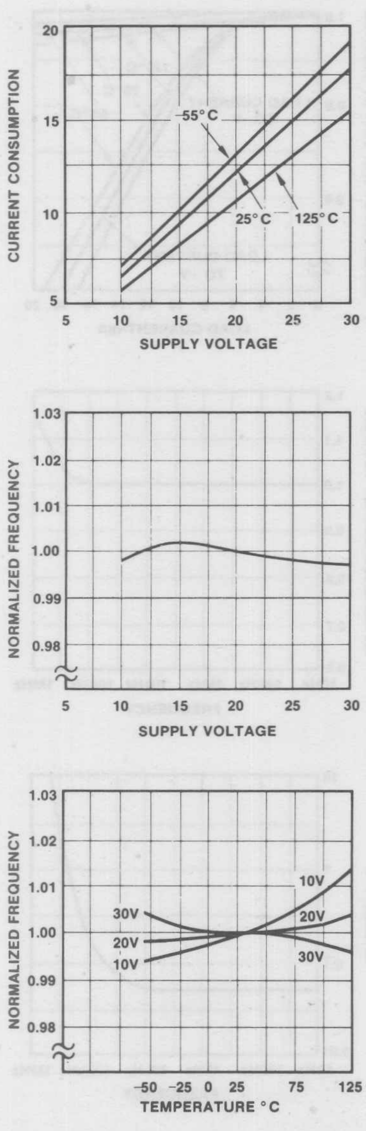

FIGURE 6. CURRENT CONSUMPTION AND FREQUENCY STABILITY.

The performance of the sine-wave output is shown in Figure 5. Figure 6 shows additional general information concerning current consumption and frequency stability and Figure 7 shows the phase relationship between the three waveforms.

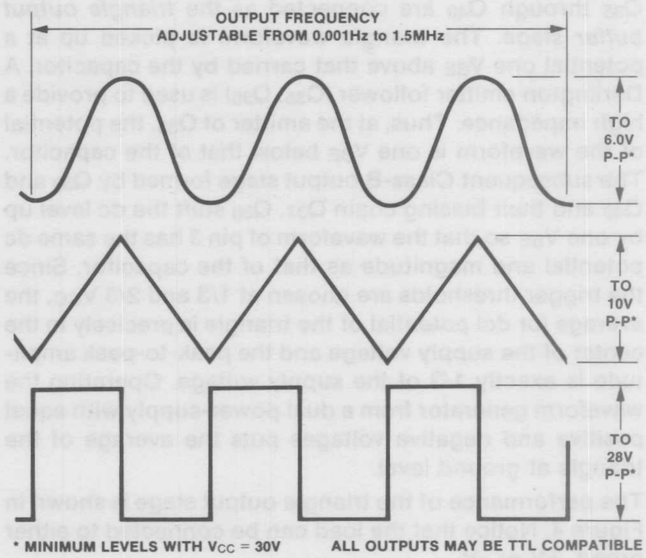

FIGURE 7. PHASE RELATIONSHIP OF WAVEFORMS.

EXTERNAL ADJUSTMENTS

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 8. By far the best result is obtained by keeping the timing resistors separate (a). R_A controls the rising portion of the triangle and sinewave and the 1 state of the square-wave. As previously discussed, the reference voltage for the two current sources is 0.2 X V_{CC}. The current therefore is simply

$$I_A = \frac{0.2 \times V_{CC}}{R_A}$$

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The magnitude of the triangle-waveform is set at 1/3 V_{CC}; therefore

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{CC} \times R_A}{1/5 \times V_{CC}} = \frac{5}{3}\ R_A \times C$$

During the falling portion of the triangle both current sources are on; the current created by R_B is doubled and I_A is subtracted from it

$$I_B = \frac{1/5 \times V_{CC}}{R_B} \times 2 - I_A$$

$$= \frac{2}{5} \times \frac{V_{CC}}{R_B} - \frac{1}{5} \times \frac{V_{CC}}{R_A}$$

and the time for the falling portion of the triangle and sinewave and the 0 state of the square wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\ V_{CC}}{\frac{2}{5} \times \frac{V_{CC}}{R_B} - \frac{1}{5} \times \frac{V_{CC}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2 R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 10% only, the connection shown in Figure 8b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 8c. This connection, however, carries an inherently larger variation of the duty-cycle, and other problems.

With two separate timing resistors, the *frequency* is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3}\ R_A C \left(1 + \frac{R_B}{2 R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.3}{R\,C} \quad \text{(for Figure 8a)}$$

It is recommended that the value of R_A and R_B be greater than 500Ω, but not more than 1MΩ.

If a single timing resistor is used (Figures 8b and c), the frequency is

$$f = \frac{0.15}{R\,C}$$

Also notice that neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear function of the supply voltage and thus their effects cancel.

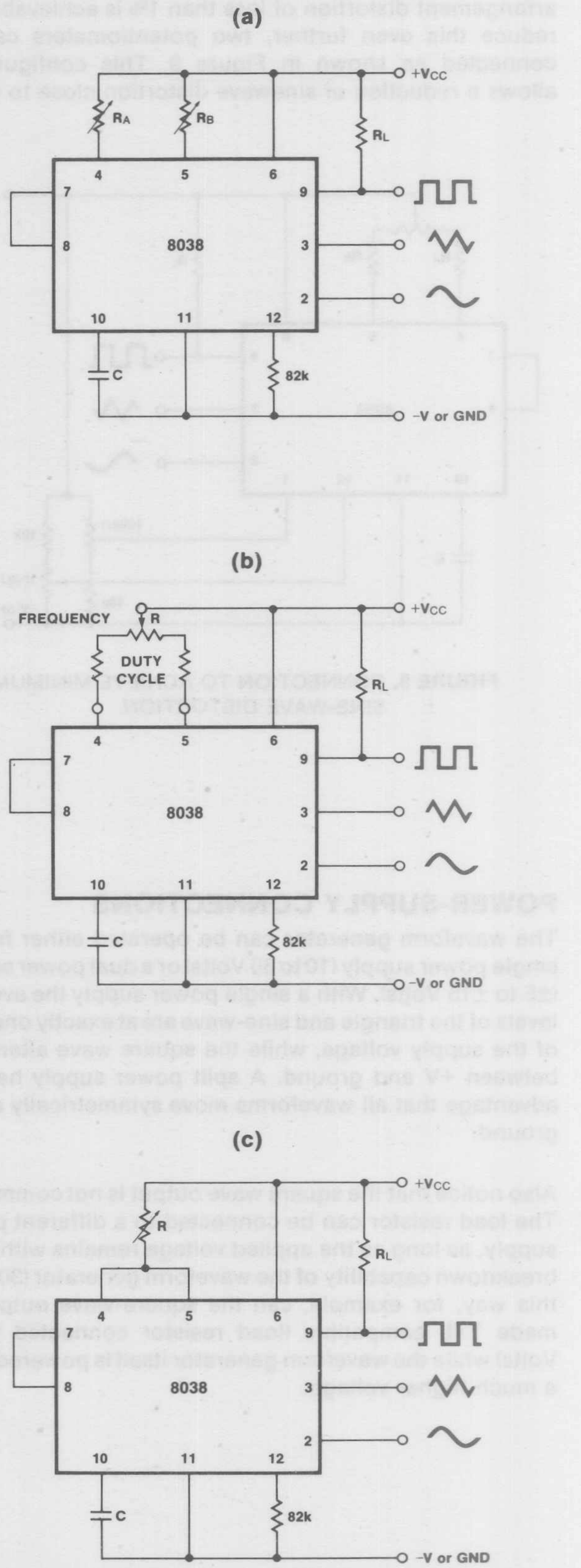

FIGURE 8. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 9. This configuration allows a reduction of sinewave distortion close to 0.5%.

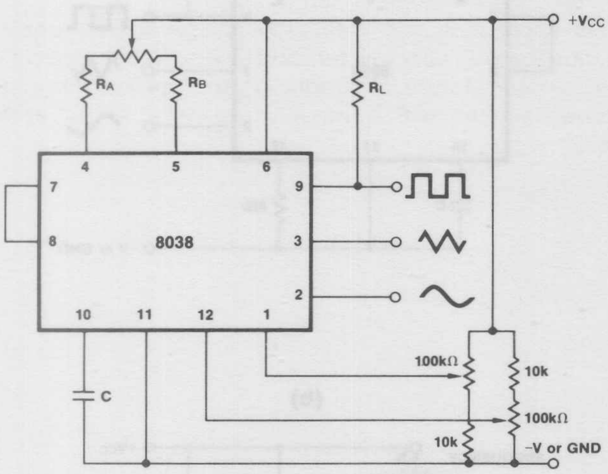

FIGURE 9. CONNECTION TO ACHIEVE MINIMUM SINE-WAVE DISTORTION.

POWER-SUPPLY CONNECTIONS

The waveform generator can be operated either from a single power supply (10 to 30 Volts) or a dual power supply (±5 to ±15 Volts). With a single power supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square wave alternates between +V and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

Also notice that the square wave output is not committed. The load resistor can be connected to a different power supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30 V). In this way, for example, can the square-wave output be made TTL compatible (load resistor connected to ±5 Volts) while the waveform generator itself is powered from a much higher voltage.

FREQUENCY MODULATION AND SWEEPING

As explained earlier, the frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from $+V_{CC}$). Thus by altering this voltage, frequency modulation is achieved.

For small deviations (i.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing dc decoupling with a capacitor, as shown in Figure 10a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance. Without it (i.e. terminals 7 and 8 connected together), the input impedance is 8kΩ; with it, this impedance increases to (R+8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 10b). In this way the entire bias for the current sources is created by the modulating signal and a very large (e.g. 1000:1) sweep range is created ($f = 0$ at $V_{sweep} = 0$). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger still are) and thus the frequency becomes dependent on the supply voltage. The potential on pin 8 may be swept from V_{CC} to about $2/3\ V_{CC} + 2V$. For example with + and −10 volt supplies, pin 8 should vary between 5.3V and +10V with respect to ground.

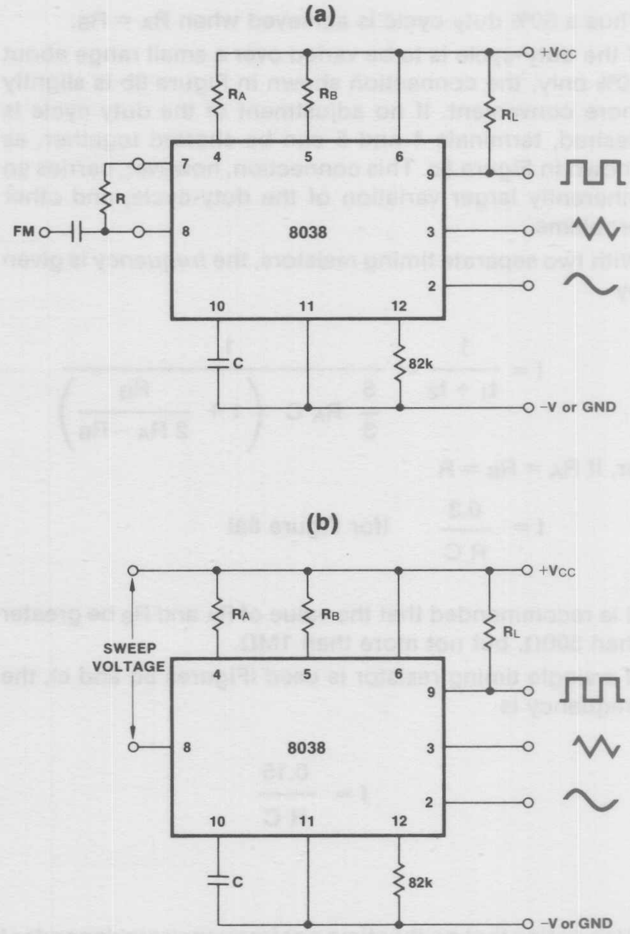

FIGURE 10. CONNECTIONS FOR FREQUENCY MODULATION (a) AND SWEEP (b).

USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the waveform generator an ideal building block for a phase-locked loop. In this application the remaining functional blocks, the phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC 4344, NE 562, HA 2800, HA 2820).

In order to match these building blocks to each other, two steps must be taken. First, if necessary, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

Second, the dc output level of the amplifier must be made compatible to the dc level required at the FM input of the waveform generator (pin 8, 0.8 x V_{CC}.) The simplest solution here is to provide a voltage divider to V_{CC} (R_1, R_2 as shown) if the amplifier has a lower output level or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

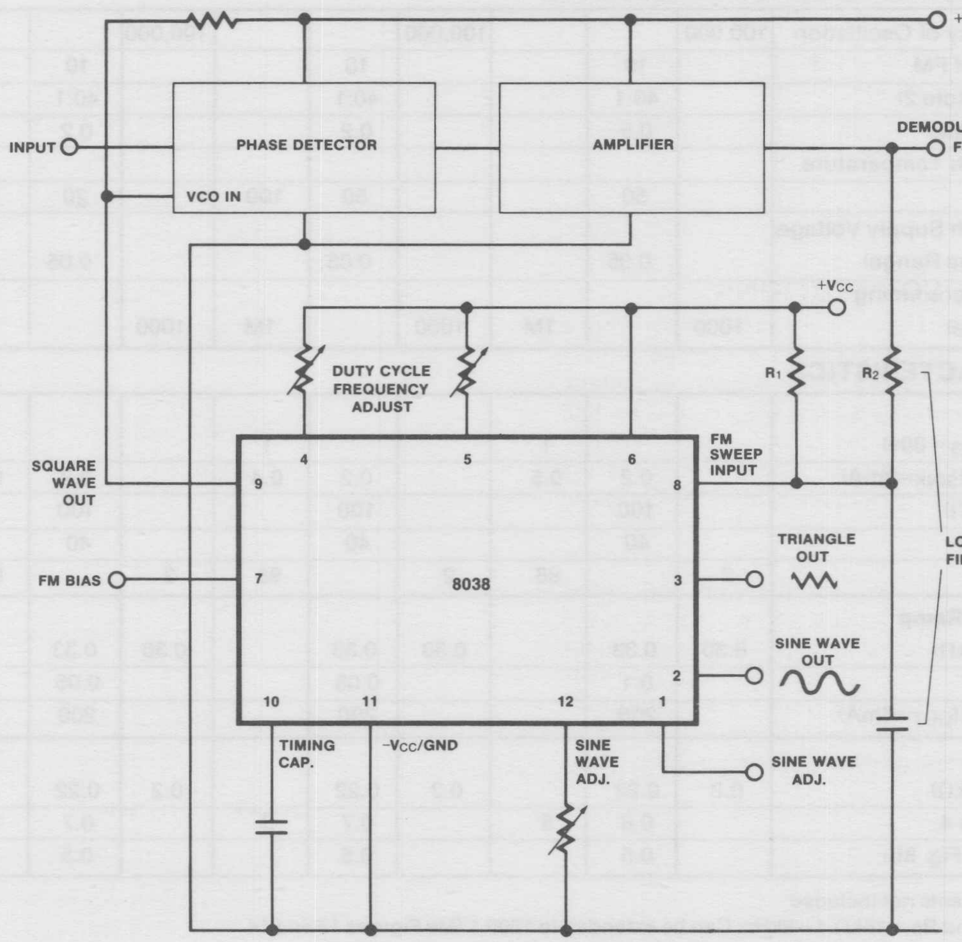

FIGURE 11. WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP.

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MAXIMUM RATINGS

Supply Voltage	±18V or 36V Total
Power Dissipation	750mW (Note 5)
Input Voltage (any pin)	Not To Exceed Supply Voltages
Input Current (Pins 4 and 5)	25 mA
Output Sink Current (Pins 3 and 9)	25 mA
Storage Temperature Range	−65° C to +125° C
Operating Temperature Range:	
8038AM, 8038BM	−55° C to +125° C
8038AC, 8038BC, 8038CC	0° C to +70° C

ELECTRICAL CHARACTERISTICS

($V_S = \pm10V$ or $+20V$, $T_A = 25°C$, $R_L = 10K\Omega$, Unless Otherwise Specified) Note 3.

	8038CC			8038BC/BM			8038AC/AM			
GENERAL CHARACTERISTICS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Supply Voltage Operating Range										
Single Supply	+10		+30	+10		30	+10		30	V
Dual Supplies	±5		±15	±5		±15	±5		±15	V
Supply Current (V_S=±10V) Note 1.										
8038AM, 8038BM					12	15		12	15	mA
8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (all waveforms)										
Maximum Frequency of Oscillation	100,000			100,000			100,000			Hz
Sweep Frequency of FM		10			10			10		kHz
Sweep FM Range (Note 2)		40:1			40:1			40:1		
FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
Frequency Drift With Temperature Note 6		50			50	100		20	50	ppm/° C
Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V_S
Recommended Programming Resistors (R_A and R_B)	1000		1M	1000		1M	1000		1M	Ω
OUTPUT CHARACTERISTICS										
Square-Wave										
Leakage Current (V_9 = 30v)			1			1			1	µA
Saturation Voltage(I_{SINK}=2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
Rise Time (R_L=4.7kΩ)		100			100			100		ns
Fall Time(R_L=4.7kΩ)		40			40			40		ns
Duty Cycle Adjust	2		98	2		98	2		98	%
Triangle/Sawtooth/Ramp										
Amplitude (R_T=100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_S
Linearity		0.1			0.05			0.05		%
Output Impedance (I_{OUT}=5mA)		200			200			200		Ω
Sine-Wave										
Amplitude (R_S=100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_S
THD(R_S=1MΩ) Note 4.		0.8	5		0.7	3		0.7	1.5	%
THD Adjusted (Use Fig. 8b)		0.5			0.5			0.5		%

NOTE 1: R_A and R_B currents not included

NOTE 2: V_S = 20V; R_A and R_B = 10kΩ, f ≅ 9kHz; Can be extended to 1000.1 See Figures 13 and 14

NOTE 3: All parameters measured in test circuit given in Fig. 2

NOTE 4: 82 kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B)

NOTE 5: Derate plastic package at 6.7 mW/° C for ambient temperatures above 50° C
Derate ceramic package at 12.5 mW/° C for ambient temperatures above 100° C

NOTE 6: Over operating temperature range, Fig. 2, pins 7 and 8 connected, V_S = ±10V. See Fig. 6c for T.C. vs V_S